A 9.5 GHz Commercially Available 1/4 GaAs Dynamic Prescaler

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Abstract—**A mass-producible 1/4 GaAs monolithic dynamic prescaler operating with a single clock input of 9.5 GHz and a power dissipation of 480 mW has been successfully realized. In addition, the phase noise performance was −100 dBc/Hz and −120 dBc/Hz at 100 Hz and 10 kHz offsets, respectively, for a 6.725 GHz input, which is considered to be low enough for practical use.**

I. Introduction

EVER SINCE the first appearance of technical work in 1974 [1], GaAs IC designers have advanced step by step, acquiring and mastering the various state-of-the-art technologies during these one and a half decades. Recently, a reliability assessment report on GaAs IC devices was presented by Katsukawa *et al.* [2], which suggests that these devices hold promise for being accepted in the market in the near future.

Many systems, especially in the microwave and gigabit fields, have stringent requirements with regard to 1) higher frequency or speed performance, 2) lower noise characteristics, 3) less turning or turning-free manufacturability, and 4) more compact size or lighter weight, in order to attain much higher quality or performance and much lower cost for the future systems. From these points of view, GaAs IC devices are expected to play a substantial role in the field applications of microwave equipment and high-speed instruments.

This paper will describe a 1/4 GaAs monolithic dynamic prescaler suitable for PLL (phase-locked loop) circuits in microwave communication and measurement systems. The developed IC can operate in single clocked fashion at a maximum frequency of 9.5 GHz. The power dissipation is as small as 480 mW with an output power of more than 0 dBm, which is large enough to drive any GaAs or Si bipolar frequency divider (e.g., two-modulus counter). In Section II, the circuit design and simulation will be discussed. Then, in Section III, a brief explanation of the basic FET and the fabrication process will be given, and in Section IV experimental results including phase noise characteristics will be reported. Finally, conclusions will be drawn in Section V.

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II. Design

When making comparisons between dynamic [3], [4] and static prescalers, the dynamic one has the following advantages:

1) the dynamic prescaler is about two times faster in operation than the static one when the same FET's are used;
2) device complexity of the dynamic prescaler is about 2/3 that of the static one, which might lead to easier fabrication and therefore a higher process yield.

With the dynamic prescaler, however, there is the disadvantage that the lower end of the operating frequency range is limited at around 1 ~ 2 GHz due to discharge current in the transfer gate FET [3].

A. Circuit Design

Fig. 1 shows a block diagram of the developed dynamic prescaler, consisting of two basic 1/2 frequency divider blocks constructed with BFL (buffered FET logic) circuits. The block includes both an inverter and a buffer amplifier, which can permit practical single clock operation and a direct cascaded configuration. The circuit design was carried out by using a modified SPICE simulation program [5].

The basic FET has such characteristics as threshold voltage (V_t) of −1 V and a gate propagation delay time (t_{pd}) of 55 ps. Fig. 2 shows the relationship between V and t_{pd} obtained from a 15-stage ring oscillator. With decreasing V_t (a more negative V_t), t_{pd} monotonically decreases to saturation, where V_t is reached at around −1 V. The dynamic prescaler bears a certain similarity in operation to the ring oscillator, and this suggests that a V_t of −1 V is the most suitable selection from the viewpoint of speed and power dissipation.

The gate width (W_g) in the inverter and the buffer portion in Fig. 1 is one of the dominant factors determining the operation speed of the dynamic prescaler. According to computer simulation with interconnect stray capacitances taken into consideration, FET sizes exceeding 60 μm have little influence on the speed improvement, mainly due to the fan-out loading effect. Based on this result, the

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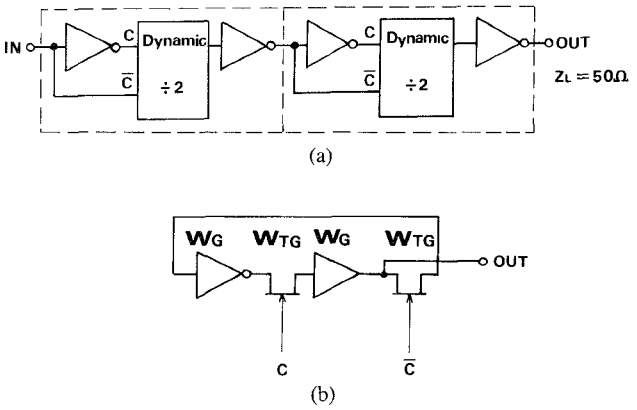


Fig. 1. 1/4 GaAs dynamic prescaler (a) Block diagram. (b) Basic 1/2 dynamic frequency divider block diagram

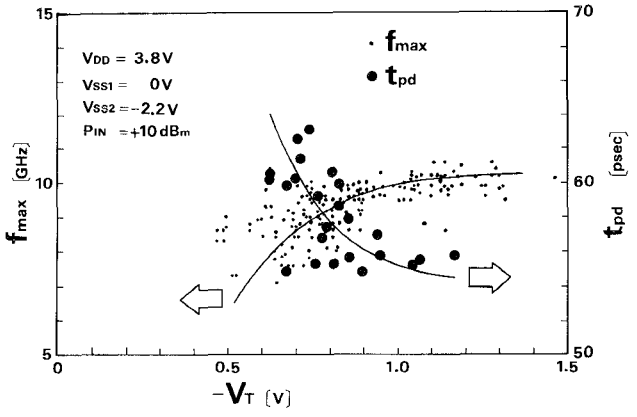


Fig. 2. The relationship between the maximum operation frequency (F_{max}) of the divider and the FET threshold voltage V_t. Measured gate delay time t_{pd} from ring oscillator measurement is also denoted on the graph.

gate width was made 50 μm for the first and 30 μm for the second 1/2 stage for speed and power optimization.

The transfer gate size (W_{tg}) is another important factor that defines the operating frequency range. Fig. 3 shows how the maximum and the minimum operating frequency (F_{max}, F_{min}) vary when W_{tg} changes. As can be seen in the figure, F_{min} drastically deteriorates when W_{tg} is over 40 μm, whereas F_{max} remains almost constant. W_{tg} was finally designed to be 30 μm for the first- and 10 μm for the second-stage 1/2 prescalers so that the maximum operating frequency range could be obtained with an allowable amount of F_{max} deterioration.

Fig. 4 shows an equivalent circuit for the single clocked dynamic 1/2 prescaler. The transfer gate bias voltage V_{GG}, as well as W_{tg}, is very sensitive to the operating frequency range. Because of this, the coupling between the prestage and the transfer gate was achieved with MIM (metal-insulator-metal) capacitors. Futhermore, the optimum voltage for wide operating frequency range was fed to the transfer gate as V_{GG}, which was made by resistors on the IC.

B. Layout

Close attention has been paid to avoid laying out IC circuit elements too near to each other and thereby incurring an undesired leakage current increase. In addition, interconnection metal as well as MIM capacitors has been formed on dielectric films such as SiO_2 or Si_3N_4, not directly on the surface of a GaAs substrate, so as to prevent the side gating effect or some extrinsic low frequency oscillation phenomena [6]-[9] from occurring through the GaAs semi-insulating substrate.

A chip photograph is shown in Fig. 5; chip size is 1.1 × 1.2 mm.

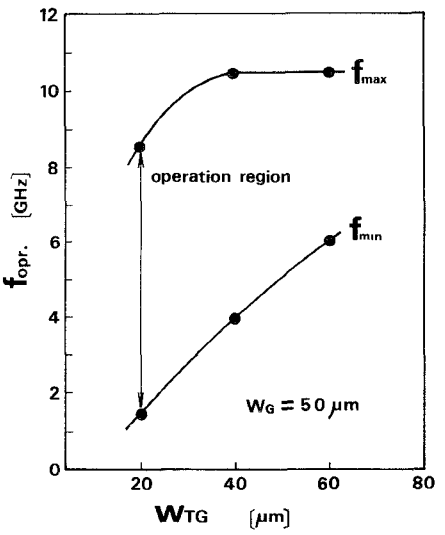


Fig. 3. Simulation results for 1/2 prescaler F_{max} and F_{min} dependencies on transfer gate FET size W_{tg}.

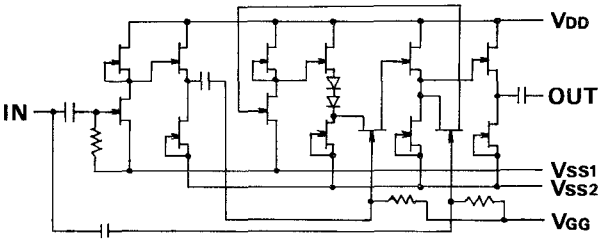


Fig. 4. Equivalent circuit for a single phase input 1/2 dynamic frequency divider

III. Fabrication

The fundamental FET used in the prescaler has a T-shaped gate of WSi refractory metal with TiN/Pt/Au on top for reducing gate resistance. Fig. 6 shows a cross-sectional view of the FET. The gate length is around 0.8 μm. Si^+ ion implantation was used to make the active layers of FET's, diodes, and resistors as well as the n^+ layers beneath the ohmic electrodes. The FET V_t was chosen to be −1 V with a transconductance (g_{m0}) of 170 mS/mm. Dry etching was utilized in the gate-slit windowing and through-hole opening. Triple layer wiring of Au was realized by using ion milling and planarization techniques.

IV. Experimental Results

A. RF Performance

Fig. 7 shows surface-mount-type, hermetically sealed, eight-pin ceramic packages for the 1/4 and 1/2 prescaler.

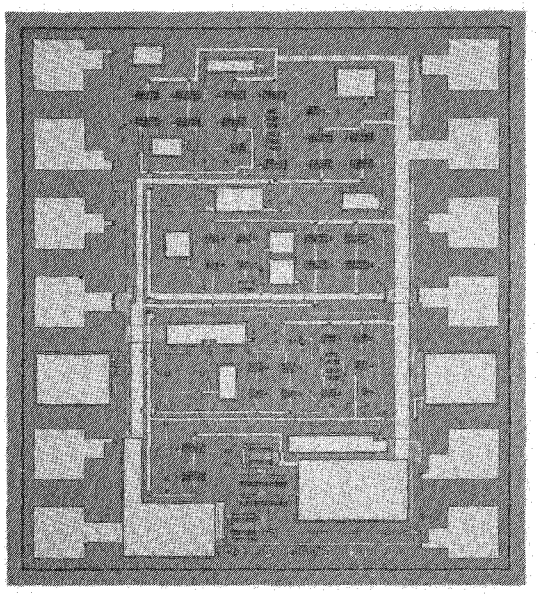


Fig. 5. The developed 1/4 prescaler chip photograph.

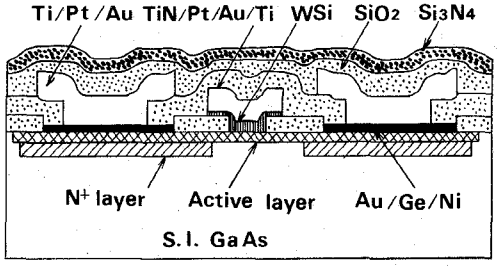


Fig. 6. A cross-sectional view of the fundamental FET.

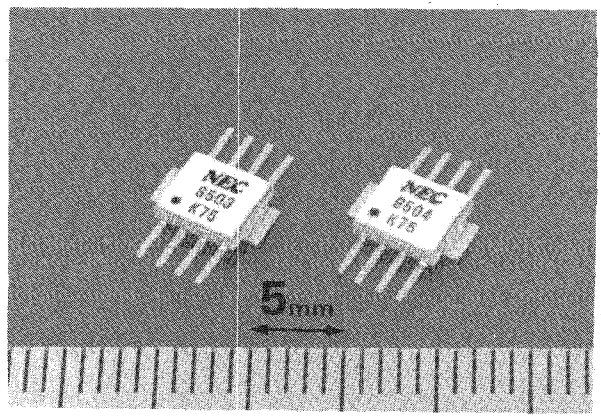
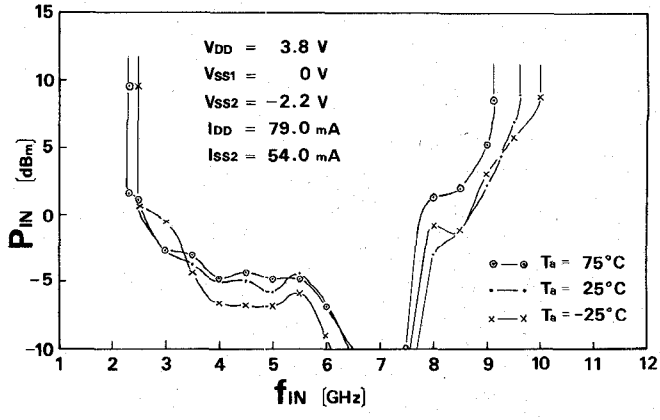
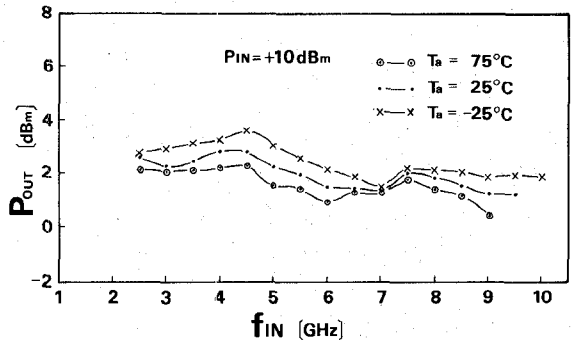


Fig. 7. The surface-mount-type, hermetically sealed, eight-pin ceramic packages (for 1/4 prescaler on left and 1/2 prescaler on right).



(a)



(b)

Fig. 8. (a) Input sensitivity curves at three different temperatures. (b) Measured 1/4 output signal levels at three different temperatures.

RF measurements were made by mounting the packaged prescaler on a RF jig. Fig. 8 shows input sensitivity versus frequency characteristics at different temperatures together with the output power behavior. As shown in Fig. 8(a), the unit exhibited a wide frequency range of operation from 2.4 to 9.6 GHz, nearly two octaves, at an input power level of +10 dBm at room temperature. At the high temperature of 75° C, F_{max} slightly decreased to 9.1 GHz with a temperature coefficient of −10 MHz/°C for a simple configuration without any temperature compensation circuit. On the other hand, F_{min} remained almost constant except at a lower input power level. Meanwhile, the output power shown in Fig. 8(b) was weakly dependent on the frequency throughout the range. It did not change more than 1 dB and resulted in +1.3 dBm at 9.5 GHz as well as +2 dBm at 8 GHz.

Fig. 2 shows an F_{max} dependency on V_t over several wafer process lots, with that of the ring oscillator t_{pd} superimposed on it. It can be seen in the figure that even less of an increase in F_{max} would be expected when V_t is less than −1 V. This partly confirms the validity of the circuit optimization procedure used for the dynamic prescaler. Fig. 9 shows F_{max} and F_{min} distributions within a wafer, evaluated by on-wafer RF probing. Sharp, high peaks indicate a fairly good uniformity of operation, and it suggests the possibility of a high operation yield. Figs. 10 and 11 shows the dynamic prescaler output in the time and frequency domains, respectively. A D/U (desired/undesired) signal ratio of about 20 dB was observed at a 2 GHz output frequency.

B. Noise Performance and Reliability

The prescaler phase noise is an important factor to be evaluated when considering practical system applications. Fig. 12 shows phase noise performances of the dynamic prescaler, obtained by making use of an HP 3048A phase noise measurement system. In Fig. 12(b), curve *A* is a noise curve of a signal source, for which an in-house high-

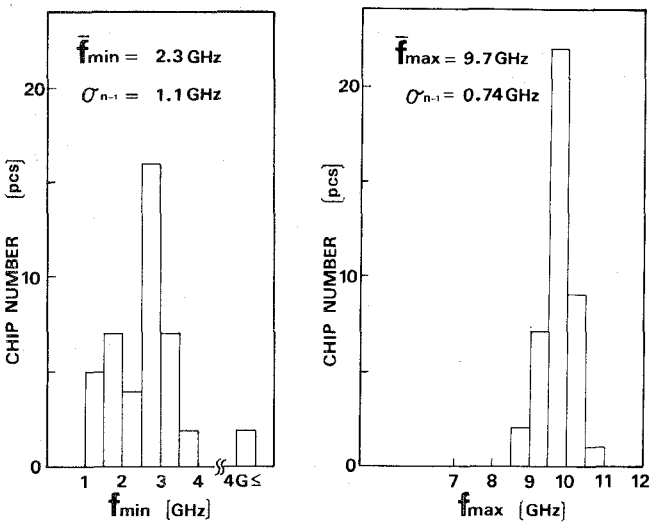
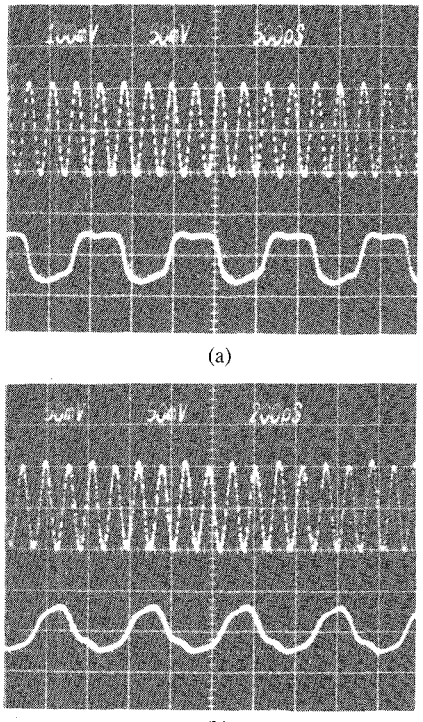


Fig. 9. Minimum operation frequency F_{min} and maximum operation frequency F_{max} distributions within a wafer.



(a)

(b)

Fig. 10. Measured 1/4 output waveforms. (a) F_{in} = 3.5 GHz, F_{out} = 0.875 GHz. (b) F_{in} = 9.0 GHz, F_{out} = 2.25 GHz.

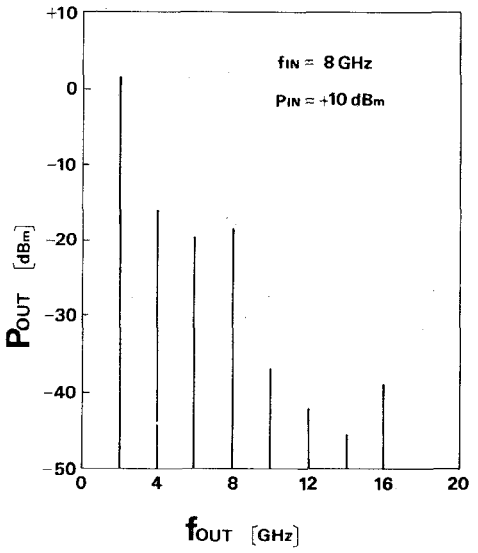
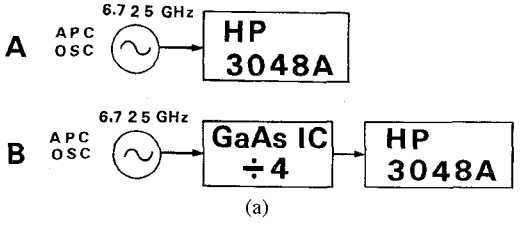
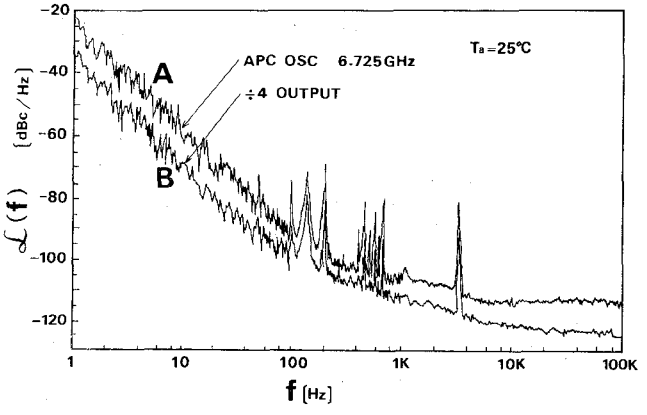


Fig. 11. Output frequency spectra for the prescaler at f_{in} = 8.0 GHz, P_{in} = +10 dBm.



(a)



(b)

Fig. 12. (a) The prescaler phase noise measurement setup. (b) A phase noise performance of the prescaler. *A* shows the phase noise of a high-purity signal source. *B* shows the phase noise of 1/4 output signal.

purity APC (automatic phase controlled) oscillator was utilized at f_{osc} = 6.725 GHz, for the purpose of preventing the inaccuracy arising from the prescaler phase noise level being covered with the source noise. Curve *B* represents an output noise curve of the 1/4 prescaler unit. The frequency spurts of the oscillator spectrum are due to the inductive coupling from the ac line (ac 100 V, 50 Hz) and its subharmonics. The spurts of the oscillator spectrum are not substrate oscillations for GaAs parts in the oscillator because no GaAs devices are used in it. (Silicon bipolar transistors and IC's are used in the APC oscillator.) As clearly seen in the figure, curve *A* can be completely overlapped on curve *B* by the 12 dB noise level reduction. This is because the prescaler reduces the sideband noise level by −12 dB ($10 \log(1/4)^2 = -12$), meaning that the prescaler works perfectly without producing any fatal noise throughout the frequency offset range of 1 Hz to 100 kHz. Furthermore, the phase noise behavior at −30°C and +75°C was also investigated and is shown in Fig. 13. There was no anomalous noise peak generated across the band of interest, and it should be noticed that the noise level is again −100 dBc/Hz and

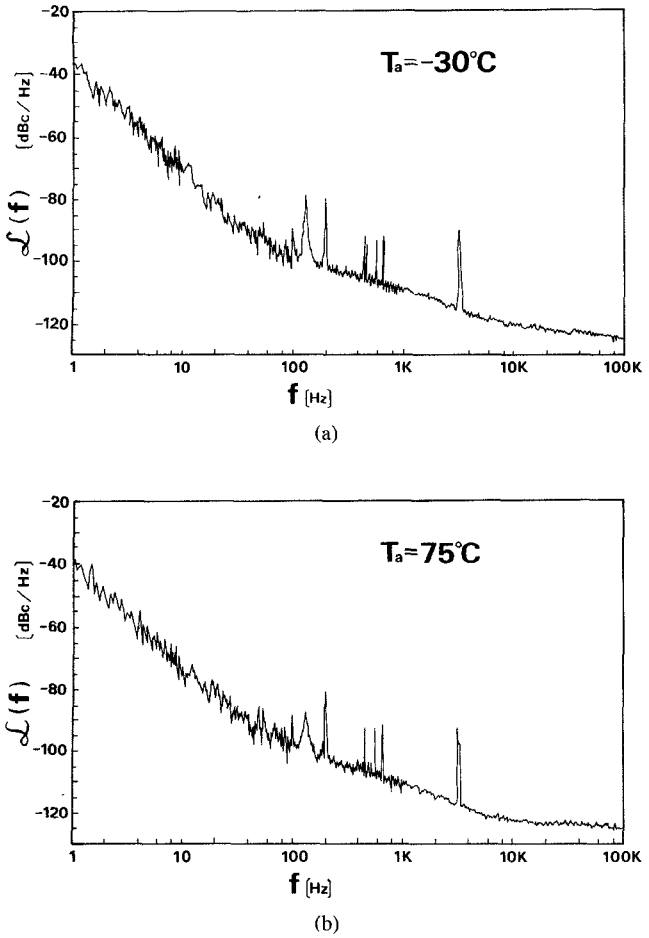


Fig. 13. The phase noise performance of the prescaler at (a) −30°C and (b) +75°C. The noise hardly varied over these ambient temperatures.

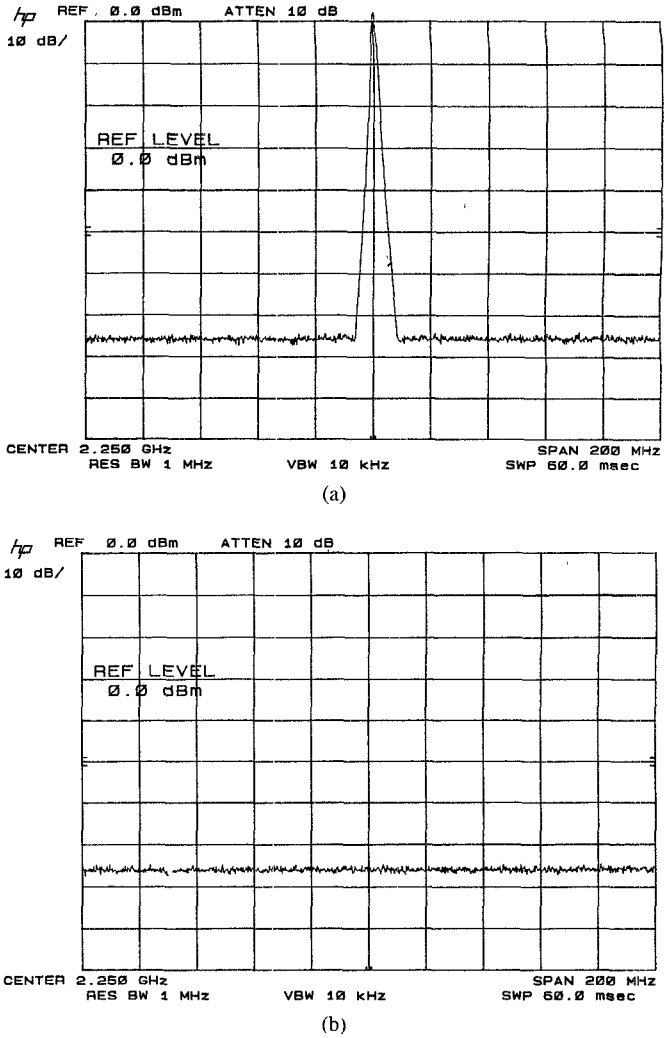


Fig. 14. (a) The 1/4 prescaler output spectrum over the range from 2.15 to 2.35 GHz at F_{in} = 9.0 GHz. (b) The noise floor of the spectrum analyzer. The measured frequency range was the same as in (a).

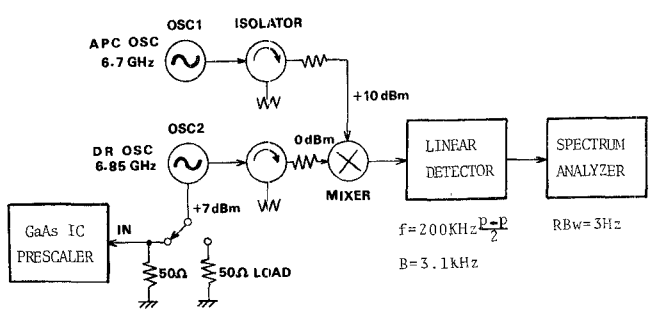


Fig. 15. A block diagram for *S/N* measurement setup of the prescaler-coupled oscillator. The OSC2 has two outputs.

−120 dBc/Hz, accomplished at 100 Hz and 10 kHz offsets, respectively, at a frequency of 6.725 GHz. Fig. 14(a) shows the output signal spectrum of the prescaler over the range of 2.15 and 2.35 GHz with a center of 2.25 GHz when the unit operates at 9 GHz. The noise floor of the spectrum analyzer is shown in Fig. 14(b). From these spectra, it can be observed that there was no increase of noise floor when the prescaler was operating.

Then, taking into consideration an actual PLL system setup, the prescaler unit is directly connected to an oscillator with a shunt 50 Ω resistor. The test setup is shown in Fig. 15. The total output noise of the oscillator (OSC2) was measured by a linear detector and a baseband spectrum analyzer for a 6.85 GHz input. Fig. 16 shows the results obtained in comparison with 50 Ω termination. The noise performance of the oscillator hardly deteriorated when the prescaler was directly coupled to the oscillator. This result shows that the prescaler can directly connect to a VCO in a PLL system without any isolators or isolation amplifiers.

The reliability is a final measure of the product completeness. Fig. 17 shows the RF burn-in testing results for the prescaler at a device junction temperature (T_j) of 115°C. F_{max} changes only a few percent over 3000 hours without any failure, meaning that the reliability potential is large enough, similar to that of the *S*-band two-stage amplifier reported previously [2].

V. Conclusion

The RF performance results described so far are summarized in Table I as well as the bias and size information. In conclusion, a single-clocked dynamic 1/4 prescaler operating at 9.5 GHz with high yields and stability was realized using a WSi gate FET, circuit simplification,

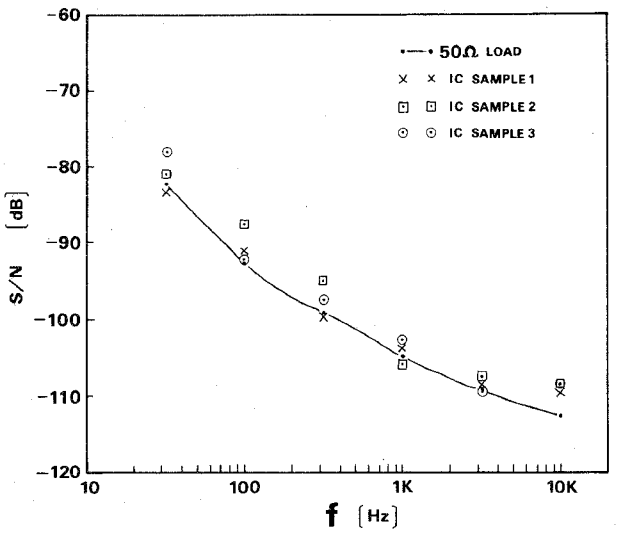


Fig. 16. *S/N* data for OSC2 when the prescaler was directly connected to OSC2 with 50 Ω shunt resistors. The solid line is a reference when only connected with 50 Ω load.

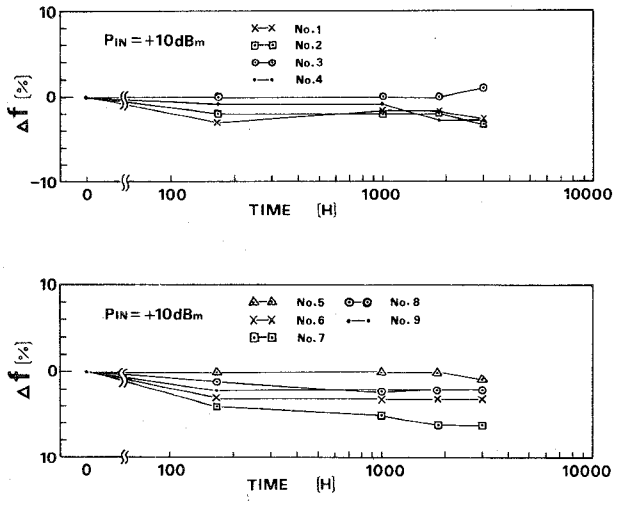


Fig. 17. RF burn-in test for the prescaler. Operation frequency was 6 GHz and input power was +10 dBm. Device junction temperature (T_j) was 115°C.

TABLE I
PERFORMANCE SUMMARY OF THE 9.5 GHz 1/4 GaAs DYNAMIC PRESCALER

Maximum Operation Freq.	9.5GHz	typ.
Minimum Operation Freq.	2.5GHz	typ.
Output Power	+3dBm	typ.
Phase Noise	Less than	−100dBc/Hz @100Hz −110dBc/Hz @1KHz −120dBc/Hz @10KHz f_{IN} = 6.725GHz
Bias Voltage : +3.8V, −2.2V		
Power Consumption : 480 mW		
Chip Size : 1.1×1.2 (t=0.14) mm		
Package Size : 5.0×4.4 (t=1.7) mm		

and design refinement. Superior noise performance was also achieved over a wide frequency offset range. The various results obtained so far will allow commercial availability of the ultra-high-speed GaAs prescaler.

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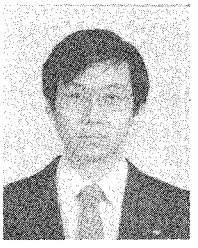

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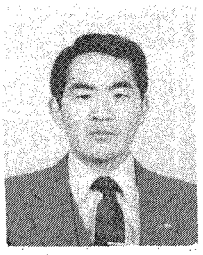

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Mr. Itoh is a member of the Institute of Electronics, Information and Communication Engineers of Japan and the Institute of the Japan Society of Applied Physics.

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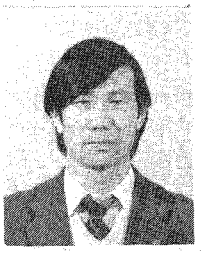

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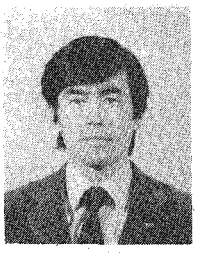

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